What is claimed is:

1. An LCD panel substrate comprising:

a gate pattern including a gate line formed on a pixel region and a peripheral region of a transparent insulating substrate respectively and a gate electrode branched from the gate line;

a gate insulating film formed the transparent insulating substrate having the gate pattern;

an active pattern formed on the gate insulating film, said active pattern including a first impurity region, a second impurity region, and a channel region formed between the first impurity region and the second impurity region;

a data pattern formed on the active pattern and the gate insulating film, said data pattern including a first electrode in contact with the first impurity region, a second electrode in contact with the second impurity region, and a data line coupled to the first electrode;

a first insulating interlayer formed on the data pattern and the gate insulating film, the first insulating interlayer having a first contact hole for partially exposing the first electrode, a second contact hole for exposing the gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing the first/second electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with the first electrode of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed first/second electrode of the second drive transistor through the second and third contact holes.

2. The LCD panel substrate of claim 1, further comprising a lower capacitor electrode formed on the pixel region of the transparent insulating substrate, the first lower capacitor electrode being made from a same layer as the gate line, the lower

capacitor electrode being spaced apart by a selected interval from the gate line and being in parallel with the gate line.

3. The LCD panel substrate of claim 1, further comprising a lower capacitor electrode formed on a gate driving region of the peripheral region of the transparent insulating substrate, said lower capacitor electrode being made from the same layer as the gate line and extending from one side edge of the gate line, the peripheral region comprising the gate driving region and a pad region.

4. The LCD panel substrate of claim 1, wherein the active pattern is comprised of amorphous silicon.

5. The LCD panel substrate of claim 1, wherein the peripheral region has a gate driving region and a pad region, and the first and second electrodes of the first and second drive transistors have an interdigital structure.

6. The LCD panel substrate of claim 1, wherein the second electrode of the second drive transistor has an upper capacitor electrode extending toward the first electrode of the first drive transistor.

7. The LCD panel substrate of claim 1, wherein the first insulating interlayer is comprised of silicon nitride.

8. The LCD panel substrate of claim 1, wherein the first insulating interlayer is comprised of a photosensitive organic insulating material.

9. The LCD panel substrate of claim 8, wherein the first insulating interlayer has an embossing formed on a surface of the first insulating interlayer.

10. An LCD panel substrate comprising:

a gate pattern including a gate line formed on a pixel region and a peripheral region of a transparent insulating substrate respectively and a gate electrode branched from the gate line;

a gate insulating film formed on the transparent insulating substrate having the gate pattern;

an active pattern formed on the gate insulating film, the active pattern including a first impurity region, a second impurity region, and a channel region formed between the first impurity region and the second impurity region;

a data pattern formed on the active pattern and the gate insulating film, said data pattern including a first electrode in contact with the first impurity region, a second electrode in contact with the second impurity region and a data line coupled to the first electrode;

a first insulating interlayer formed on the data pattern and the gate insulating film, the first insulating interlayer including a first contact hole for partially exposing the second electrode, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing the gate electrode of a first drive transistor of the peripheral region, and a fourth contact hole for exposing the first/second electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern coupled to the second electrode of the pixel region through the first contact hole, a second electrode pattern coupled to the first electrode of the pixel region through the second contact hole, and a third electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed first/second electrode of the second drive transistor through the third and fourth contact holes.

11. The LCD panel substrate of claim 10, further comprising a lower capacitor electrode formed on the pixel region of the transparent insulating substrate, said lower capacitor electrode being made from a same layer as the gate line, and the lower capacitor electrode being spaced apart by a selected interval from the gate line

and being in parallel with the gate line.

12. The LCD panel substrate of claim 10, further comprising a lower capacitor electrode formed on a gate driving region of the peripheral region of the transparent insulating substrate, said lower capacitor electrode being made from a same layer as the gate line and extending from one side edge of the gate line, the peripheral region having the gate driving region and a pad region.

13. The LCD panel substrate of claim 10, wherein the active pattern is comprised of amorphous silicon.

14. The LCD panel substrate of claim 10, wherein the peripheral region includes a gate driving region and a pad region, and the first and second electrodes of the first and second drive transistors have an interdigital structure.

15. The LCD panel substrate of claim 14, wherein the second electrode of the second drive transistor has an upper capacitor electrode extending toward the first electrode of the first drive transistor.

16. The LCD panel substrate of claim 10, wherein the first insulating interlayer is comprised of silicon nitride.

17. The LCD panel substrate of claim 10, wherein the first insulating interlayer is comprised of a photosensitive organic insulating material.

18. The LCD panel substrate of claim 17, wherein the insulating interlayer has an embossing formed on a surface of the insulating interlayer.

19. The LCD panel substrate of claim 10, wherein all the first, second and third electrode patterns are comprised of a same material.

20. A method for manufacturing an LCD panel substrate, comprising the steps of:

forming a gate pattern including a gate line and a gate electrode branched from the gate line on a pixel region and a peripheral region of a transparent insulating substrate ;

sequentially forming a gate insulating film, a non-doped amorphous silicon layer, an impurity-doped amorphous silicon layer, and a metal layer on the insulating substrate having the gate pattern;

forming a photoresist pattern on the metal layer, the photoresist pattern having a portion which corresponds to a channel region between a source electrode and a drain electrode and is thinner than other portions corresponding to the source electrode and the drain electrode;

patterning the exposed metal layer, the impurity-doped amorphous silicon layer, and the non-doped amorphous silicon layer using the photoresist pattern as a mask to remove the metal layer of the channel region and to form a data pattern including the source electrode, the drain electrode spaced apart from the source electrode, and a data line coupled to the drain electrode and substantially perpendicular to the gate line;

removing the photoresist pattern and the impurity-doped amorphous silicon layer of the channel region;

forming an insulating interlayer on a resultant structure of the substrate;

forming a first contact hole for partially exposing the drain electrode of the pixel region, a second contact hole for exposing the gate electrode of a first transistor of the peripheral region, and a third contact hole for exposing the source/drain electrode of a second transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the insulating interlayer having the first, second, and third contact holes; and

forming a first electrode pattern and a second electrode pattern by patterning the conductive film, the first electrode pattern being coupled to the drain electrode of the pixel region through the first contact hole, and the second electrode pattern connecting

the partially exposed gate electrode of the first transistor with the exposed source/drain electrode of the second transistor through the second and third contact holes.

21. The method of claim 20, the step of forming the photoresist pattern comprising the sub-steps of:

forming a photoresist film on the metal layer;

exposing the photoresist film to a light, wherein a portion between the source electrode region and the drain electrode region on the metal layer and a first portion except for the source electrode region and the drain electrode region are exposed to a first depth which is a depth for full exposure and a second portion is exposed to a second depth lower than the first depth, the second portion including the portion between the source electrode region and the drain electrode region and the source electrode region and the drain electrode region; and

developing and removing the exposed first and second portions of the photoresist film.

22. The method of claim 20, wherein the non-doped amorphous silicon layer, the impurity-doped amorphous silicon layer, and the metal layer are formed by a PECVD (plasma enhanced chemical vapor deposition) method.

23. The method of claim 21, wherein the photoresist film is a positive type photoresist film, and the photoresist pattern is formed using a mask having a transparent region and an opaque region, the mask having slits formed at transparent regions between the channel region and the source region, and between the channel region and the drain region.

24. The method of claim 20, wherein at least one of the exposed metal layer, the impurity-doped amorphous silicon layer, and the non-doped amorphous silicon layer is removed by a dry etch method such that the photoresist pattern of the second portion is removed together when the metal layer exposed during the step of forming the data

pattern, the impurity-doped amorphous silicon layer, and the non-doped amorphous silicon layer are removed.

25. The method of claim 20, wherein the insulating interlayer is comprised of an inorganic insulating material or an organic insulating material.

26. The method of claim 20, wherein both the first and second electrode patterns are comprised of ITO or IZO.

27. The method of claim 20, wherein both the first and second electrode patterns are comprised of opaque metal film and the insulating interlayer is comprised of a photosensitive organic insulating layer having an embossing structure at a surface thereof.

28. A method for manufacturing an LCD panel substrate, comprising the steps of:

forming a gate pattern including a gate line and a gate electrode branched from the gate line on a pixel region and a peripheral region of a transparent insulating substrate respectively;

sequentially forming a gate insulating film, a non-doped amorphous silicon layer, an impurity-doped amorphous silicon layer, and a metal layer on the transparent insulating substrate having the gate pattern;

forming a photoresist pattern on the metal layer, wherein an upper surface of a channel region between a source electrode and a drain electrode is leveled lower than an upper surface of each of the source electrode and the drain electrode;

patterning the metal layer, the impurity-doped amorphous silicon layer, and the non-doped amorphous silicon layer using the photoresist pattern as a mask for removing the metal layer of the channel region and for forming a data pattern including the source electrode and the drain electrode spaced apart from the source electrode;

removing the photoresist pattern and the impurity-doped amorphous silicon layer

of the channel region;

forming an insulating interlayer on a resultant structure of the substrate;

forming a first contact hole for partially exposing the drain electrode of the pixel region, a second contact hole for partially exposing the source electrode of the pixel region, a third contact hole for exposing the gate electrode of a first transistor of the peripheral region, and a fourth contact hole for exposing the source/drain electrode of a second transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the insulating interlayer having the first, second, third and fourth contact holes; and

forming a first electrode pattern, a second electrode pattern, and a third electrode pattern by patterning the conductive film, the first electrode pattern being coupled to the source electrode of the pixel region through the first contact hole, the second electrode pattern being coupled to the drain electrode of the pixel region through the second contact hole, and the third electrode pattern connecting the exposed gate electrode of the first transistor with the exposed source/drain electrode of the second transistor through the third and fourth contact holes.

29. The method of claim 28, the step of forming the photoresist pattern comprising the sub-steps of:

forming a photoresist film on the metal layer;

exposing the photoresist film to a light, wherein a portion between the source electrode region and the drain electrode region on the metal layer and a first portion except for the source electrode region and the drain electrode region are exposed to a first depth which is a depth for full exposure and a second portion is exposed to a second depth lower than the first depth, the second portion including the portion between the source electrode region and the drain electrode region and the source electrode region and the drain electrode region; and

developing and removing the exposed first and second portions of the photoresist film.

30. The method of claim 28, wherein the non-doped amorphous silicon layer, the impurity-doped amorphous silicon layer and the metal layer are formed by a PECVD method.

31. The method of claim 29, wherein the photoresist film is a positive type photoresist film, and the photoresist pattern is formed using a mask having a transparent region and an opaque region, the mask having slits formed at transparent portions of the transparent region between the channel region and the source region, and the transparent region between the channel region and the drain region.

32. The method of claim 28, wherein at least one of the metal layer, the impurity-doped amorphous silicon layer and the non-doped amorphous silicon layer is removed by a dry etch method such that the photoresist pattern of the second portion is removed together when the metal layer exposed during the step of forming the data pattern, the impurity-doped amorphous silicon layer and the non-doped amorphous silicon layer are removed.

33. The method of claim 29, wherein the insulating interlayer is comprised of an inorganic insulating material or an organic insulating material.

34. The method of claim 29, wherein all the first, second, and third electrode patterns are comprised of ITO or IZO.

35. The method of claim 29, wherein all the first, second, and third electrode patterns are comprised of an opaque metal and the insulating interlayer is a photosensitive organic insulating film having an embossing at a surface thereof.

36. A method for manufacturing an LCD panel substrate, comprising the steps of:

forming a gate pattern including a gate line and a gate electrode branched from

the gate line on a pixel region and a peripheral region of a transparent insulating substrate;

forming a gate insulating film on the transparent insulating substrate having the gate pattern;

forming an active pattern on the gate insulating film, the active pattern including a first impurity region, a second impurity region, and a channel region between the first impurity region and the second impurity region;

forming a data pattern including a drain electrode placed on and in contact with the first impurity region, a source electrode being placed on and making contact with the second impurity region, and a data line coupled to the source electrode and substantially perpendicular to the gate line;

forming an insulating interlayer on the data pattern and the gate insulating film;

forming a first contact hole for partially exposing the drain electrode of the pixel region, a second contact hole for exposing the gate electrode of a first drive transistor of the peripheral region and a third contact hole for exposing the source/drain electrode of a second drive transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the insulating interlayer having the first, second, and third contact holes; and

forming a first electrode pattern and a second electrode pattern by patterning the conductive film, the first electrode pattern being coupled to the drain electrode of the pixel region through the first contact hole and the second electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed source/drain electrode of the second drive transistor through the second and third contact holes.

37. The method of claim 36, wherein the gate pattern is formed on the pixel region of the transparent insulating substrate, said gate pattern being made from a same layer as the gate line, and including a first lower capacitor electrode which is spaced apart by a predetermined interval from the gate line and is in parallel with the gate line and a second lower capacitor electrode which is formed on the peripheral

region of the transparent insulating substrate and is extending from one side of the gate line.

38. The method of claim 36, wherein the peripheral region comprises a gate driving region and a pad region, and the data pattern of the gate driving region comprises the source and drain electrodes of the first and second drive transistors, the source and drain electrodes having an interdigital structure.

39. The method of claim 38, wherein the drain electrode of the first drive transistor of the gate driving region has an upper capacitor electrode extending toward the source electrode of the second drive transistor.

40. A method for manufacturing an LCD panel substrate, comprising the steps of:

forming a gate pattern including a gate line and gate electrode branched from the gate line on a pixel region and a peripheral region of a transparent insulating substrate;

forming a gate insulating film on the insulating substrate having the gate pattern;

forming an active pattern on the gate insulating film, the active pattern including a first impurity region, a second impurity region and a channel region between the first impurity region and the second impurity region;

forming a data pattern including a drain electrode which is placed on and makes contact with the first impurity region, a source electrode which is placed on and makes contact with the second impurity region and a data line coupled to the source electrode and substantially perpendicular to the gate line;

forming an insulating interlayer on the data pattern and the gate insulating film;

forming a first contact hole for partially exposing the source electrode of the pixel region, a second contact hole for partially exposing the drain electrode of the pixel region, a third contact hole for exposing the gate electrode of a first transistor of the peripheral region and a fourth contact hole for exposing the source/drain electrode of a

second transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the first insulating layer having the first, second, third, and fourth contact holes; and

forming a first electrode pattern, a second electrode pattern, and a third electrode pattern by patterning the conductive film, the first electrode pattern being coupled to the source electrode of the pixel region through the first contact hole, the second electrode pattern being coupled to the drain electrode of the pixel region through the second contact hole and the third electrode pattern connecting the exposed gate electrode of the first transistor with the exposed source/drain electrode of the second transistor through the third and fourth contact holes.

41. The method of claim 40, wherein the gate pattern is formed on the pixel region of the transparent insulating substrate and is made from a same layer as the gate line, and comprises a first lower capacitor electrode spaced apart by a predetermined interval from the gate line and parallel to the gate line and a second lower capacitor electrode formed on the peripheral region of the substrate and from the same layer as the gate line and extending from one side of the gate line.

42. The method of claim 40, wherein the peripheral region comprises a gate driving region and a pad region, and the data pattern of the gate driving region comprises the source and drain electrodes of the first and second drive transistors, the source and drain electrodes having an interdigital structure.

43. The method of claim 42, wherein the drain electrode of the first drive transistor of the gate driving region has an upper capacitor electrode extending toward the source electrode of the second drive transistor.